Digital Design

CSCE 2114-L007

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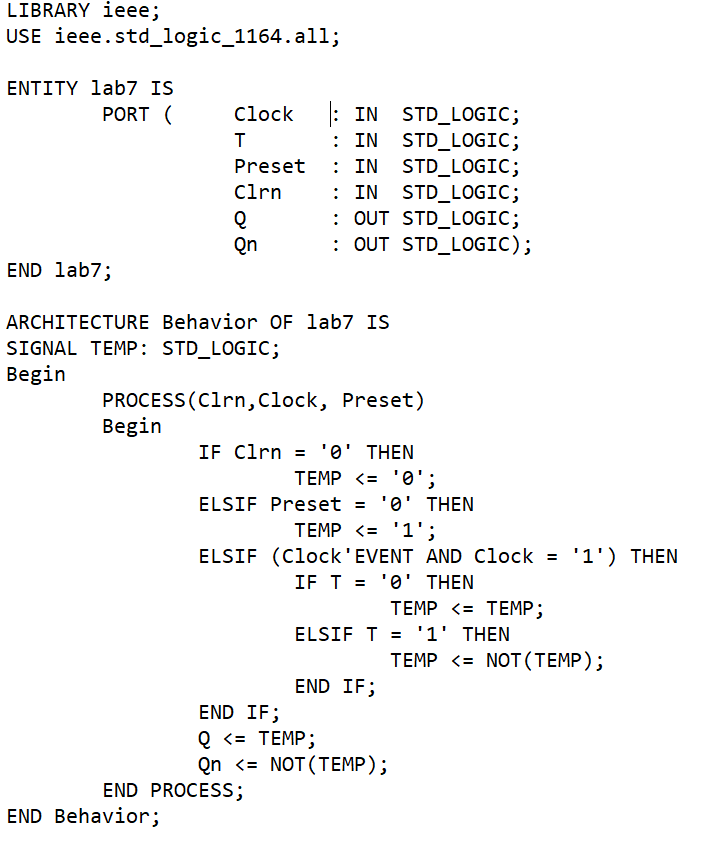
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**Introduction**

This lab went over how to write VHDL code from scratch on how to implement a rising edge triggered T flip-flop that has an asynchronous active low clear input and an asynchronous active low preset input. In a T flip-flop, the Q output is only changed on the rising edge of the clock whenever T is equal to 1, otherwise Q will remain unchanged. Since this is asynchronous then Q will not change exactly on the rising edge of the clock but will change when T is equal to 1. Since there is a clear input, anytime it is equal to 0 the input Q is equal to 0. With the preset input, anytime that is equal to 1 then the input Q is equal to 1.

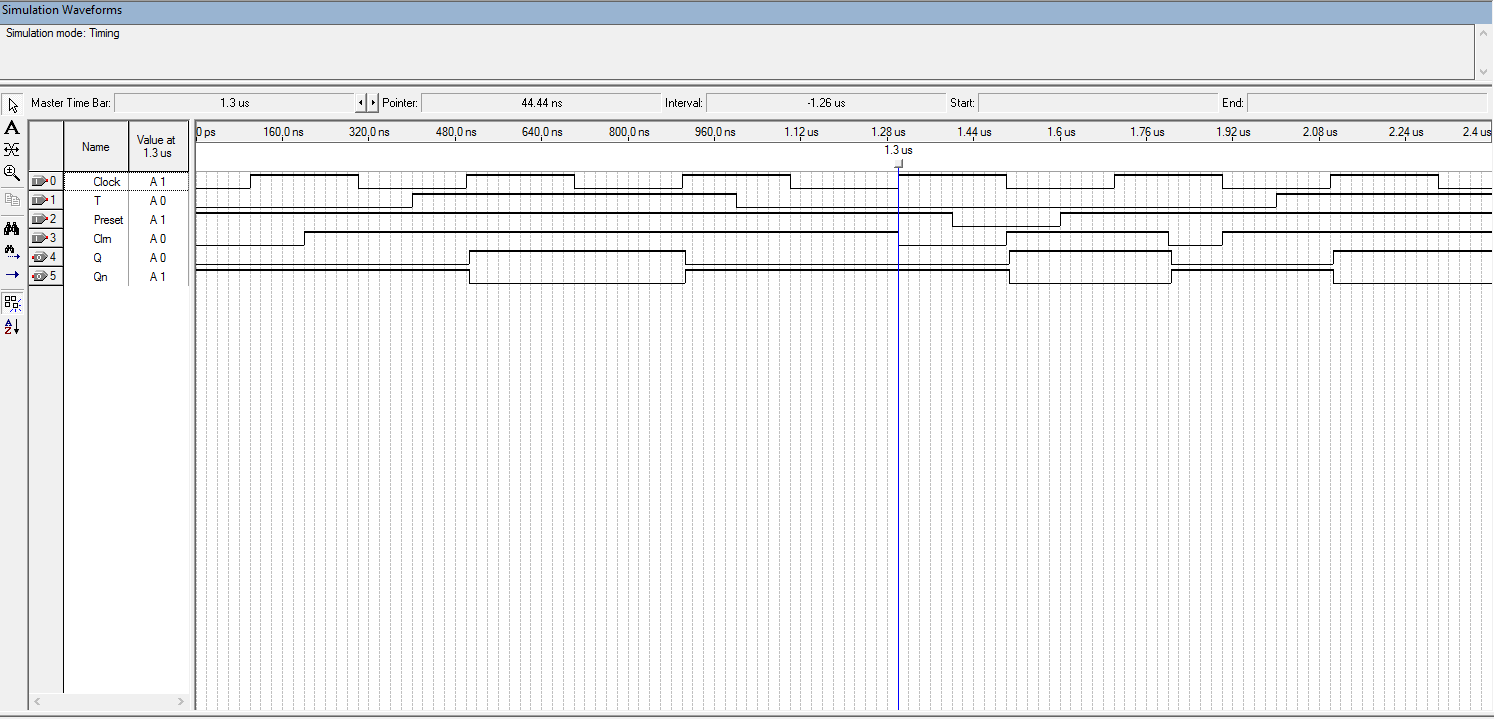
**Design**

No sample code was given and had to be written from scratch but the notes could be referred to for help. In the VHDL code, there are four inputs, Clock, T, Preset, and Clear, and there are two outputs, Q and the invert of Q. Three of the inputs were used in the process, Clear, Clock, and Preset. In the process, there are a series of if statements and if Clear is equal to 0 then Q is forced to a 0 or if Preset is equal to 0 then Q is equal to 1. On the rising edge of the Clock if T is equal to 0 the value of Q does not change otherwise Q is equal to the invert of Q. The variable Q could not be used in the series of if statements so a temporary variable was used in place of Q and was set equal to Q after the if statements with the invert of Q being set equal to the invert of the temporary variable. A picture of the VHDL code is shown below.



**Results**

The results are as shown below. As shown in the vector waveform that was made from the VHDL code above, just because the clock value changed to a 1 the input Q will only change when both the clock value and T are a 1. The input Q is forced to a 0 if the clear value is a 0 and Q is also forced to a 1 if the preset is equal to 0.



**Conclusion**

Building a T flip-flop using only the notes seemed like a challenge but once all broken down into parts it made this lab a lot simpler. Since Q only changed on the rising edge of the clock if T was equal to 1 and Q would be forced to a 0 if the input clear was equal to 0 if just showed that this was nothing more than a series of if statements.